Refclk Fanout Best Practices for 8GT/s and 16GT/s Systems

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Disclaimer

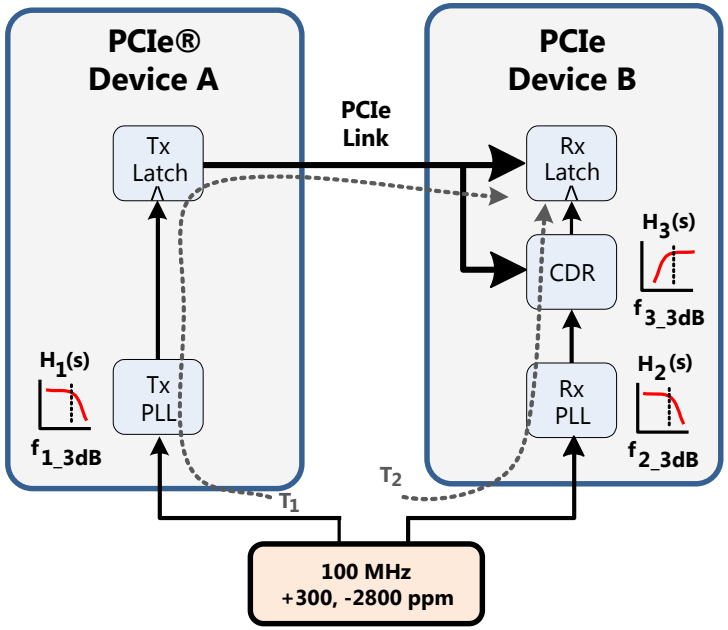
<u>Presentation Disclaimer</u>: All opinions, judgments, recommendations, etc. that are presented herein are the opinions of the presenter of the material and do not necessarily reflect the opinions of the PCI-SIG®.

Agenda

- **Clock Architectures and Jitter Filters**
  - Common Clock (CC)
  - Separate Reference (SRIS/SRNS)
- **Clock Jitter Budgets**
  - 8GT/s
  - 16GT/s
- **Clock Fanout Architectures**
  - Single Plane or Connector
  - Cascaded Connector
- **Cascading Buffers**
  - Zero Delay Buffers
  - Fixed Delay Buffers
- **Accurate Jitter Measurements**
  - Sampling Scope Noise
  - Phase Noise Analyzer
- **Optimized Clock Routing**
  - Microstrip vs. Stripline
  - Long Trace Signal Integrity
  - Coupled Noise
- **Conclusion**

Common Clock Architecture

- **Clock phase noise is filtered:**
  - Band pass by transmit and receive PLL BW difference,
  - High pass by CDR BW (CDR tracks low frequency jitter),
  - Up to 6dB boost by delay (at F=1/T /2, 180 degrees out of phase)
- **Jitter filter assumes max delay (T=12ns) and min/max PLL BW**
  - 64 combinations



Tx PLL $$H_1(s) = \frac{2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}{s^2 + 2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}$$

Rx PLL $$H_2(s) = \frac{2 \cdot s \cdot \zeta_2 \cdot \omega_{n2} + \omega_{n2}^2}{s^2 + 2 \cdot s \cdot \zeta_2 \cdot \omega_{n2} + \omega_{n2}^2}$$

CDR $$H_3(s) = \frac{s}{s + \omega_{n3}}$$

Refclk Path Delay Difference: $T = |T1 - T2|$

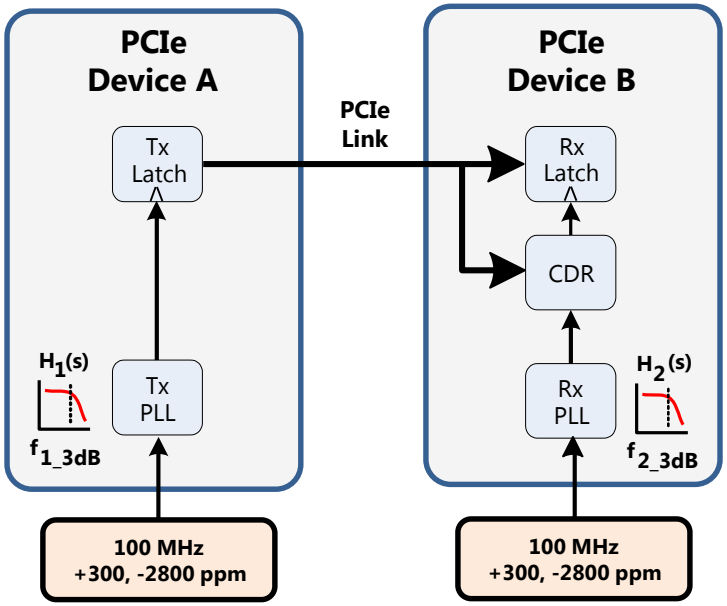
Overall Transfer Function

$$H(s) = \left(H_1(s) \cdot e^{-s \cdot T} - H_2(s)\right) \cdot H_3(s)$$

$$H'(s) = \left(H_2(s) \cdot e^{-s \cdot T} - H_1(s)\right) \cdot H_3(s)$$

SRNS/SRIS Clock Architecture

- **Clock phase noise is filtered:**
  - Band pass by PLLs BW (max BW/peak is worst case)
  - High pass by CDR BW (CDR tracks low frequency jitter)
- **Independent paths add RMS**
- **Special CDR for SRIS**



$$H_1(s) = \frac{2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}{s^2 + 2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}$$

$$H_2(s) = \frac{2 \cdot s \cdot \zeta_2 \cdot \omega_{n2} + \omega_{n2}^2}{s^2 + 2 \cdot s \cdot \zeta_2 \cdot \omega_{n2} + \omega_{n2}^2}$$

$$H_{CDR}(s) = \frac{s^2}{s^2 + s \cdot A + B} \times \frac{s^2 + 2 \cdot \zeta_2 \cdot \omega_0 \cdot s + \omega_0^2}{s^2 + 2 \cdot \zeta_1 \cdot \omega_0 \cdot s + \omega_0^2} \times \frac{s}{s + \omega_{n1}}$$

Since the reference clocks are independent of each other and given that their dominant jitter is random, then their combined impact on the system should be root sum square of the individual terms.

$$X_{SRIS} = \sqrt{[X_1(s) \times H_1(s) \times H_{CDR}(s)]^2 + [X_2(s) \times H_2(s) \times H_{CDR}(s)]^2}$$

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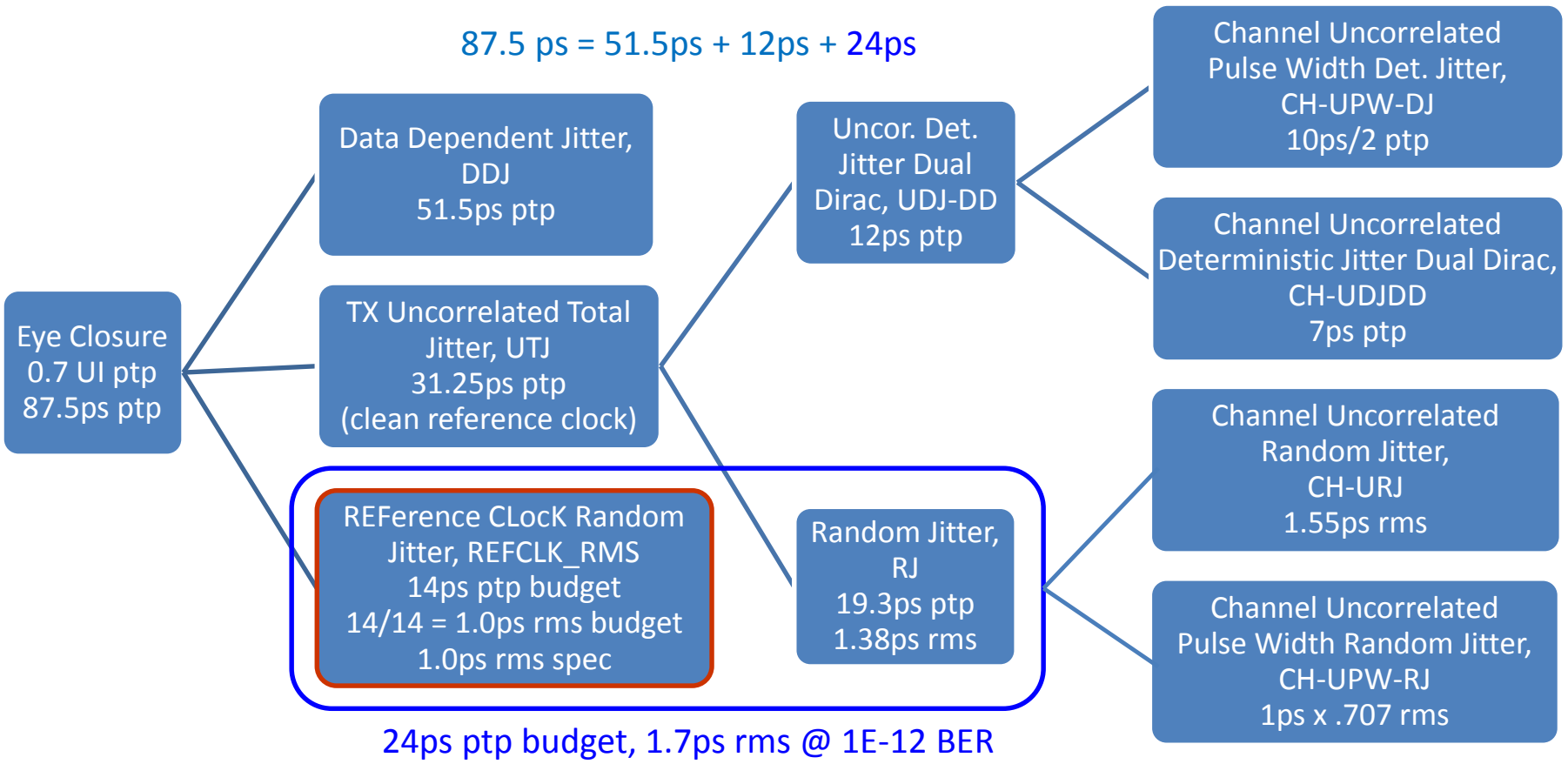
Clock Jitter Specs

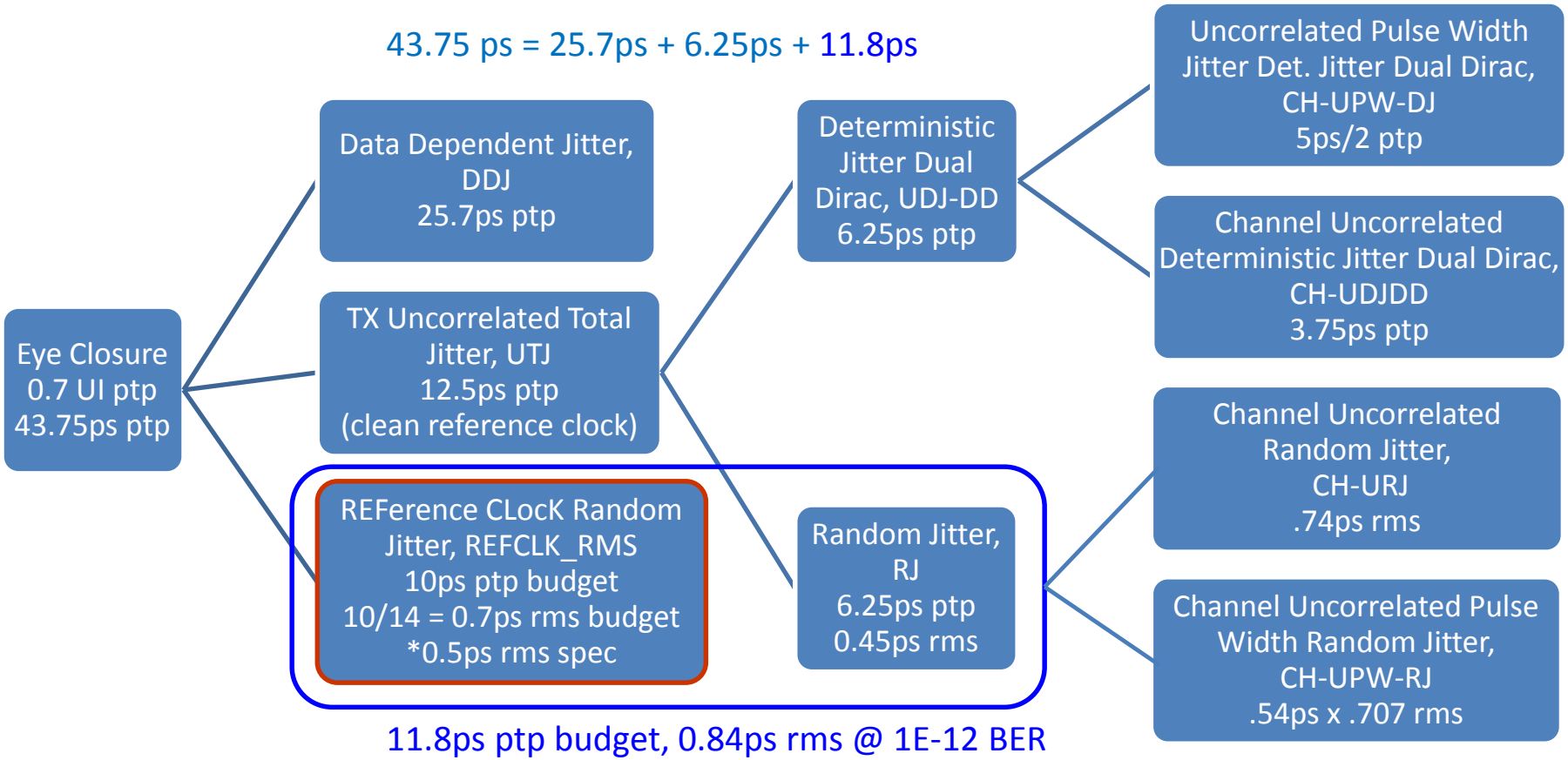
Arch.	Elect Spec	TX/RX PLL BW, Ord, PK max	Dly (ns)	CDR BW, Ord, PK max	Jitter Limit for 10^{-12} BER (ps rms)	
					8GT/s	16GT/s
Common Clock	3.1	2-4MHz, 2nd, .01-2dB 2-5MHz, 2nd, .01-1dB	12	10MHz, 1st, 0dB	1.0	n/a
	4.0 v0.9	2-4MHz, 2nd, .01-2dB 2-5MHz, 2nd, .01-1dB	12	10MHz, 1st, 0dB	1.0	**0.5***
Data Clock	3.1	4MHz, 2nd, 2dB 5MHz, 2nd, 1dB	n/a	10MHz, 1st, 0.5-2dB	1.0	n/a
Separate Ref. No Spread	3.1	4MHz, 2nd, 2dB 5MHz, 2nd, 1dB	n/a	No spec (10MHz, 1st, 3dB)	No spec (1.0/sqrt2 ea)	n/a
Sep. Ref. Indep. Spread	3.1	4MHz, 2nd, 2dB	n/a	'10MHz, 2nd, 1dB' ~6MHz & 400kHz	0.5 each (1.0/sqrt2 ea)	n/a
	4.0 v0.9	2-4MHz, 2nd, .01-2dB 2-5MHz, 2nd, .01-1dB (4MHz, 2nd, 2dB)	n/a	'10MHz, 2nd, 1dB & 400kHz,1st' ~6MHz & 400kHz	No spec (1.0/sqrt2 ea)	No spec (0.7/sqrt2 ea)

***Specified at 0.5ps rms, but channel simulations use 0.7ps rms for system noise margin**

8GT/s TX Jitter Budget



16GT/s TX Jitter Budget



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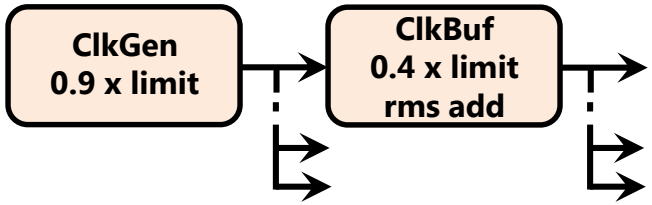
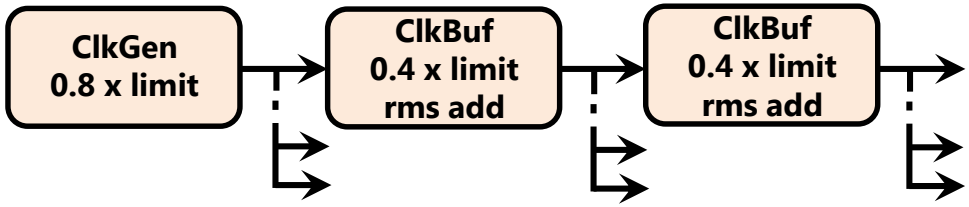
Clock Fanout Architectures

- **Typical config**
  - ClkGen – Buffer – connector – load
  - 0.98 = sqrt (0.9^2 + 0.4^2) or sqrt(0.95^2 + 0.3^2)

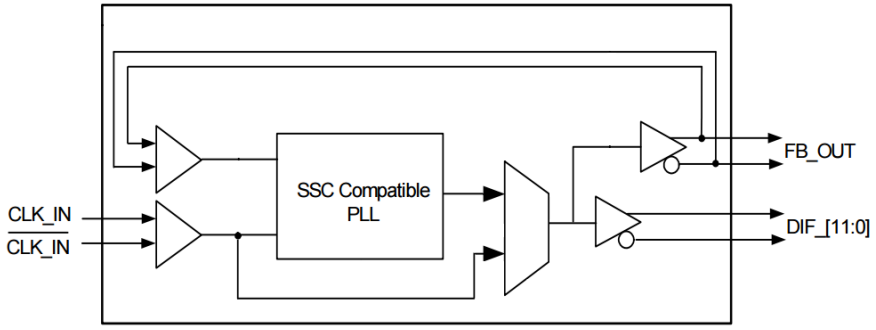


- **Worst case config**
  - ClkGen – connector – Buffer – con/cable/con – Buffer – load
  - 0.98 = sqrt (0.8^2 + 0.4^2+0.4^2)
  - 0.99 = sqrt (0.9^2 + 0.3^2 + 0.3^2)



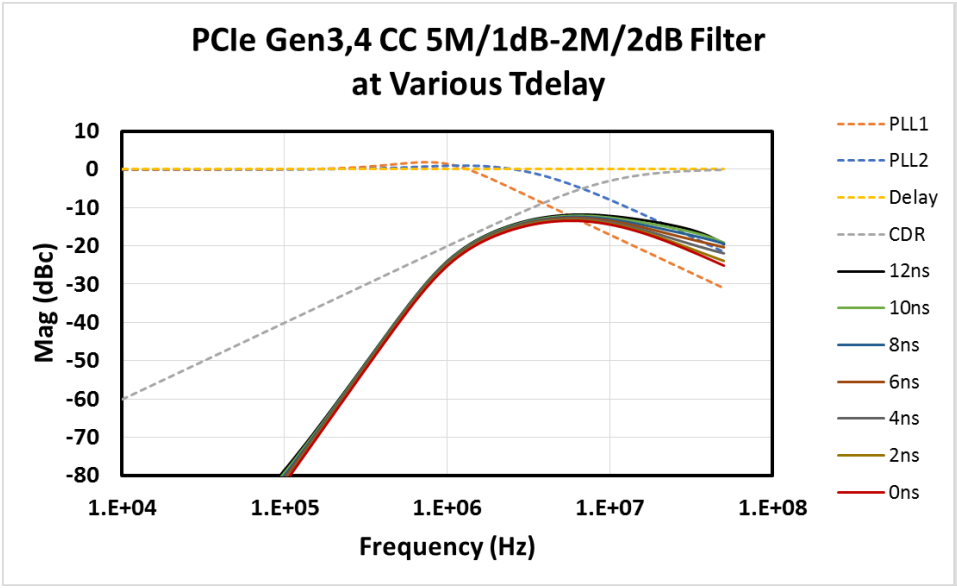
Types of Clock Buffers

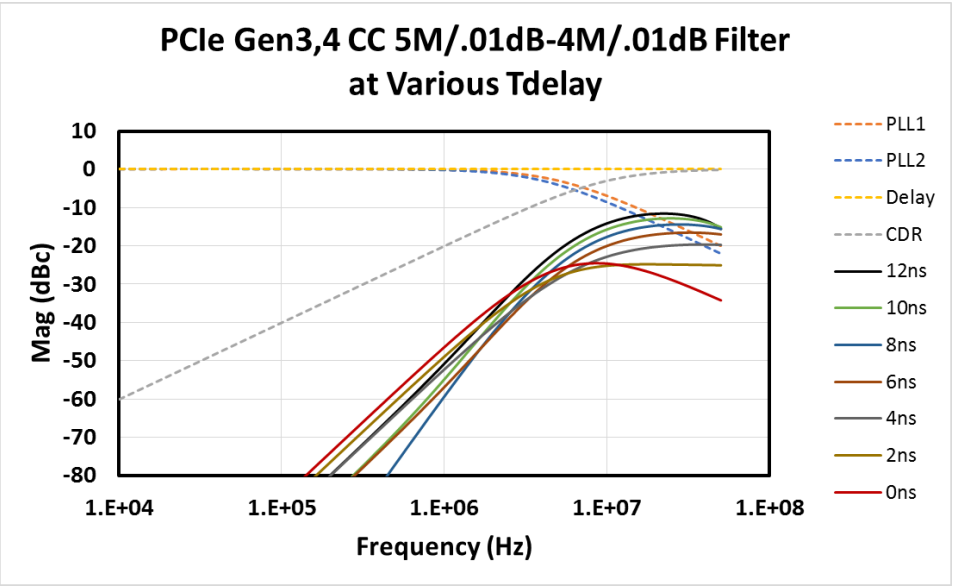
- **Zero Delay Buffer (ZDB)**
  - PLL or DLL Band Width (BW) filters jitter and adds rms
  - Higher additive jitter (loop phase noise and jitter peaking)
  - Does NOT add to clock path delay (+/-100ps)
- **Fixed Delay Buffer (or ZDB in 'pass through')**
  - No PLL, passes all jitter in PCIe band then adds rms
  - Lower additive jitter
  - DOES add to clock path delay (typically 3-4ns max)



Buffer Jitter vs. Delay Tradeoff

- **ZDB additive jitter is 2-4x pass through jitter**
  - Jitter disadvantage, +6dB to +12dB (less if in cascade…stay tuned)
  - Delay advantage, -3dB at high frequencies (12 -> 8ns)
  - 12ns is specified filter delay





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Cascading Zero-Delay Buffers

- **All components**
  - Jitter within the ZDB loop BW adds rms
  - BW must be high enough to track spread (>29*Fmod)
- **Final component**
  - ZDB jitter outside the ZDB loop BW adds rms

	Clock	1st ZDB	2nd ZDB
Low Freq. rms (in band)	Jcl	Jzl	Jzl
High Freq. rms (out of band)	Jch	Jzh	Jzh
Total component rms	Jct=sqrt(Jcl^2+Jch^2)	Jzt=sqrt(Jzl^2+Jzh^2)	Jzt
Total cascaded rms		Jz1=sqrt(Jcl^2 +Jzl^2+Jzh^2)	Jz2=sqrt(Jcl^2 +Jzl^2 +Jzl^2+Jzh^2)

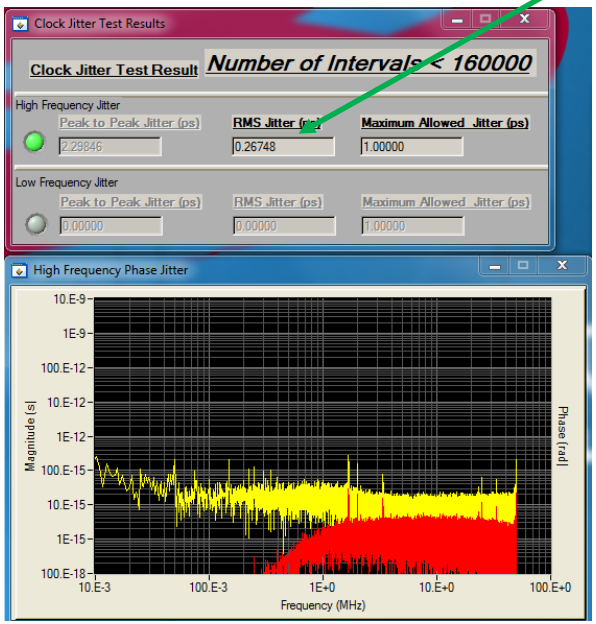
Add rms

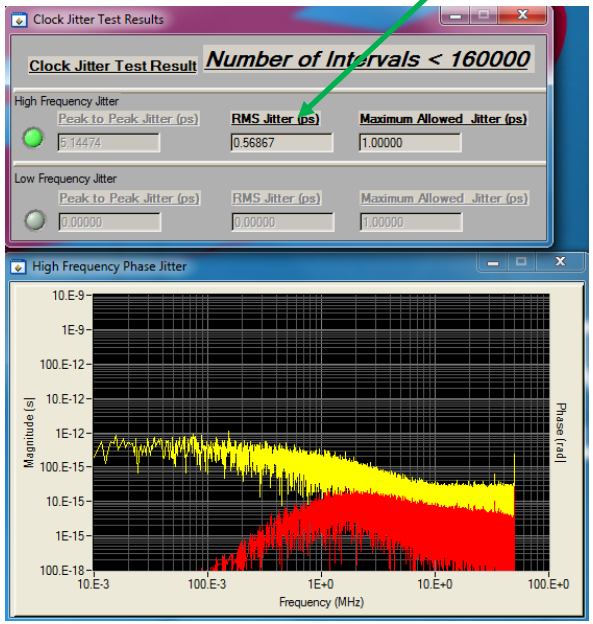
ZDB jitter usually specified as a single number, Jz1 or additive = sqrt(Jz1^2 – Jct^2)
Therefore measure or assume worst case, sqrt(Jz1^2 + Jz1^2)

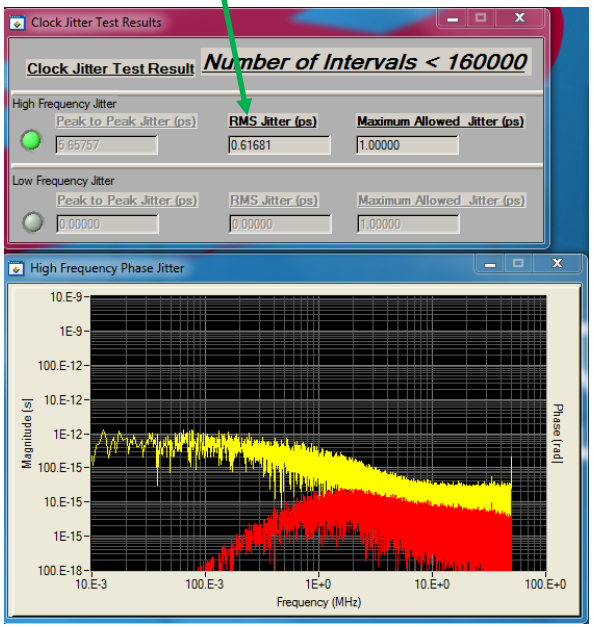
8GT/s Cascaded ZDB Example Si53112 Low BW (~1MHz)

	Clock	1st ZDB	2nd ZDB
Low Freq. ps rms	0.08	0.24	0.24
High Freq. ps rms	0.26	0.51	0.51
Total component ps rms	0.27	0.56	0.56
Total cascaded ps rms		0.57	0.62

Add rms

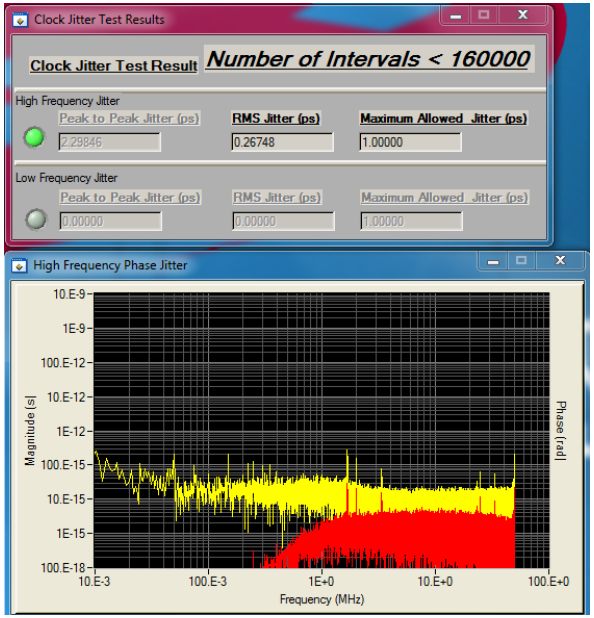


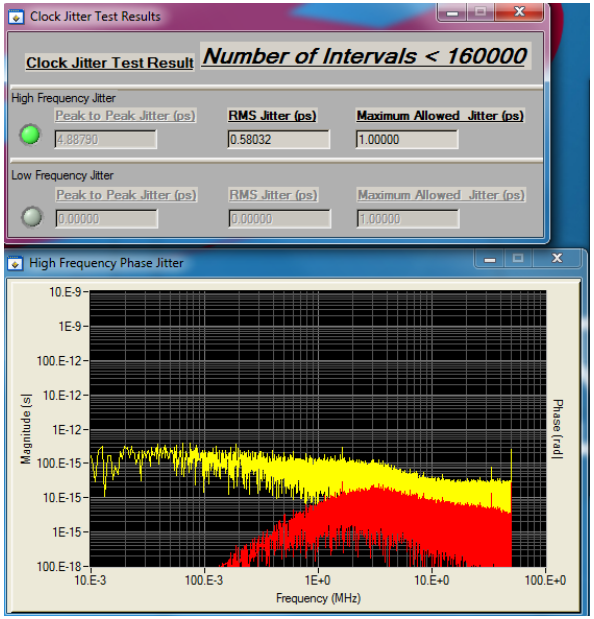


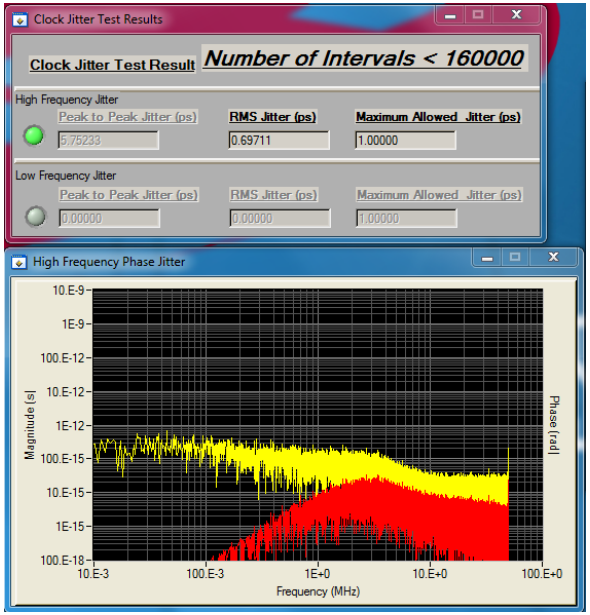


8GT/s Cascaded ZDB Example Si53112 High BW (~3MHz)

	Clock	1st ZDB	2nd ZDB
Low Freq. ps rms	0.10	0.40	0.40
High Freq. ps rms	0.25	0.41	0.41
Total component ps rms	0.27	0.57	0.57
Total cascaded ps rms		0.58	0.70







Cascading Fixed Delay Buffers

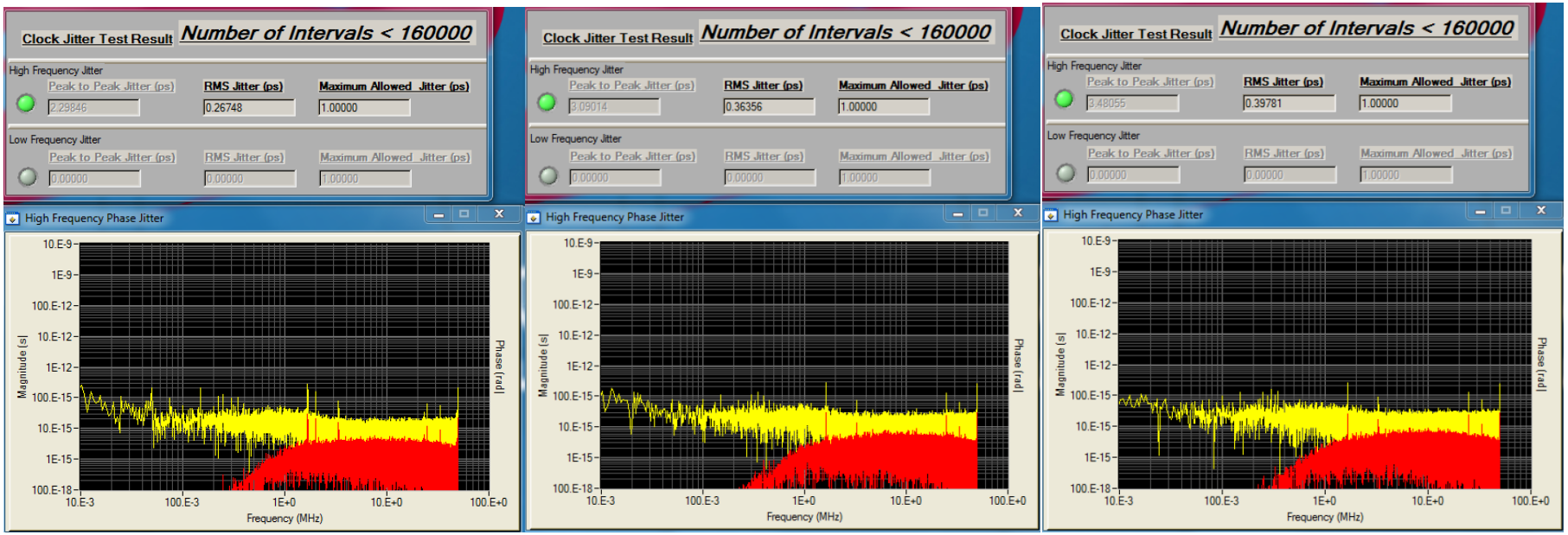
- **Fixed delay buffer jitter adds rms**
- **Propagation delay adds directly to path**

	Clock	1st ZDB	2nd ZDB
Total component rms	Jc	Jb	Jb
Total cascaded rms		Jb1=sqrt(Jc^2 +Jb^2)	Jb2=sqrt(Jc^2 +Jb^2 +Jb^2)

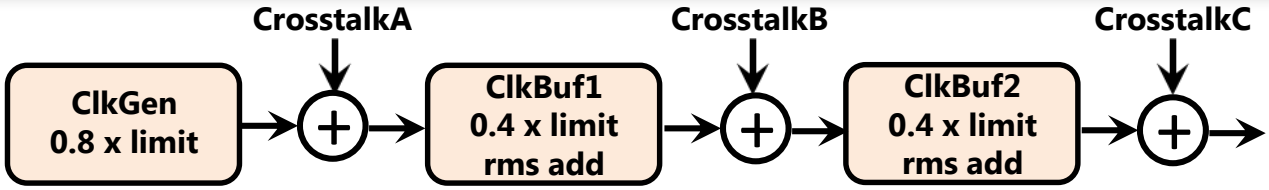
Add rms

16GT/s Cascaded Example
Si53112 Fixed Delay (Pass Through)

	Clock	1st Buffer	2nd Buffer
Total component ps rms	0.27	0.23	0.23
Total cascaded ps rms		0.36	0.42



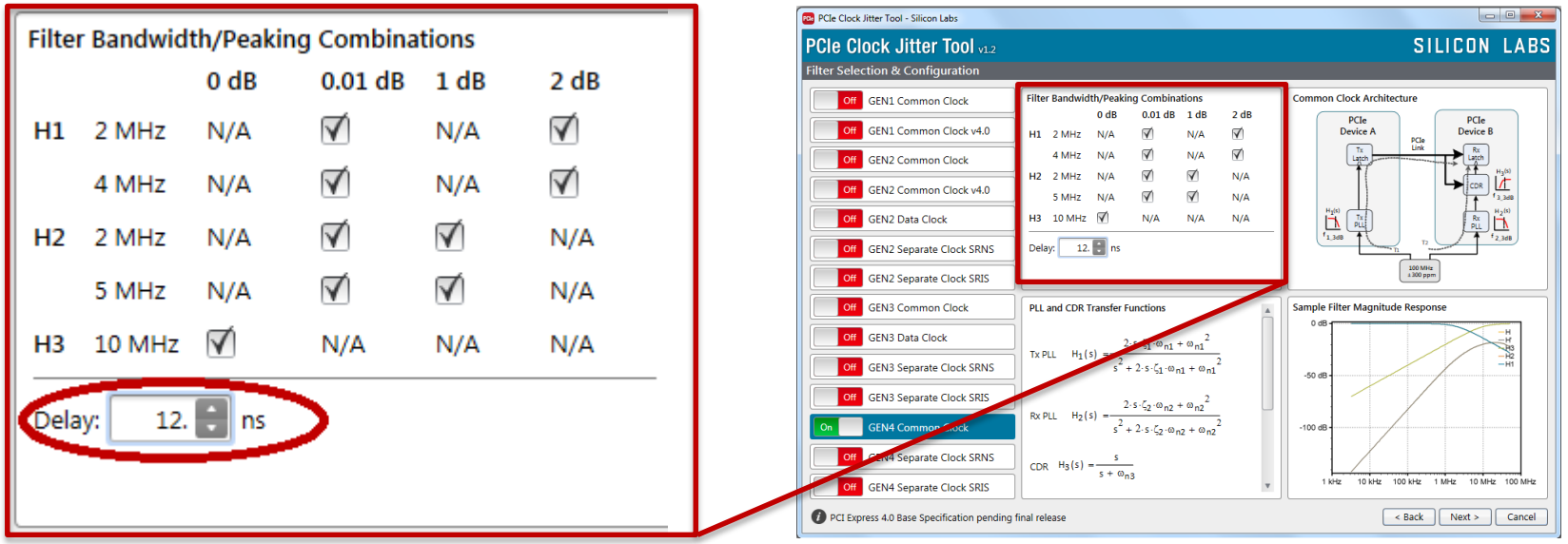
ZDB vs. Fixed Delay Example



Jitter Source	Type	ZDB w/ Fbw			Fixed Delay	
		Effect	M.ps	Ex.ps	Effect	Ex.ps
ClkGen	rms	In band only	0.3	0.4	All additive	0.4
CrosstalkA	det	Pass < Fbw	1.0	1.0	All pass	1.0
ClkBuf1	rms	In band only	0.3	0.4	All additive	0.2
CrosstalkB	det	Pass < Fbw	1.0	1.0	All pass	1.0
ClockBuf2	rms	All additive	0.4	0.4	All additive	0.2
CrosstalkC	det	All pass	1.0	1.0	All pass	1.0
Tdelay adjust		Lower	-3dB	0dB	Nominal	0dB
Total rms (0.5ps max)	rms	0.58 w/o T adj	0.41	0.69		0.49
Total ptp (10ps budg)	ptp	11.2 w/o T adj	8.8	12.7		9.9

ZDB vs. Fixed Delay Buffer

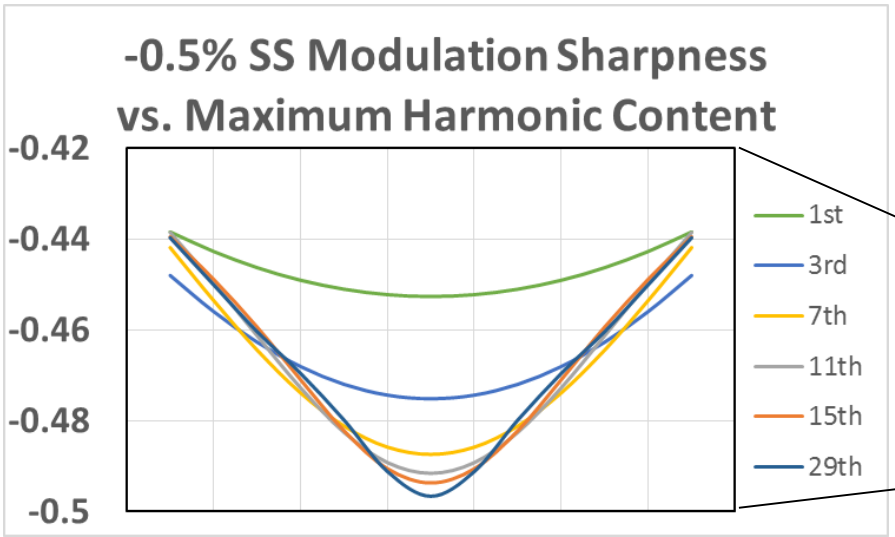
- **Use of ZDB can be beneficial IF**
  - Willing to measure in cascade to determine BW effects
  - Willing to factor in reduced Tdelay in PCIe jitter filter
- **Otherwise Fixed Delay provides lowest jitter**
- **Some jitter tools allow adjustable Tdelay**

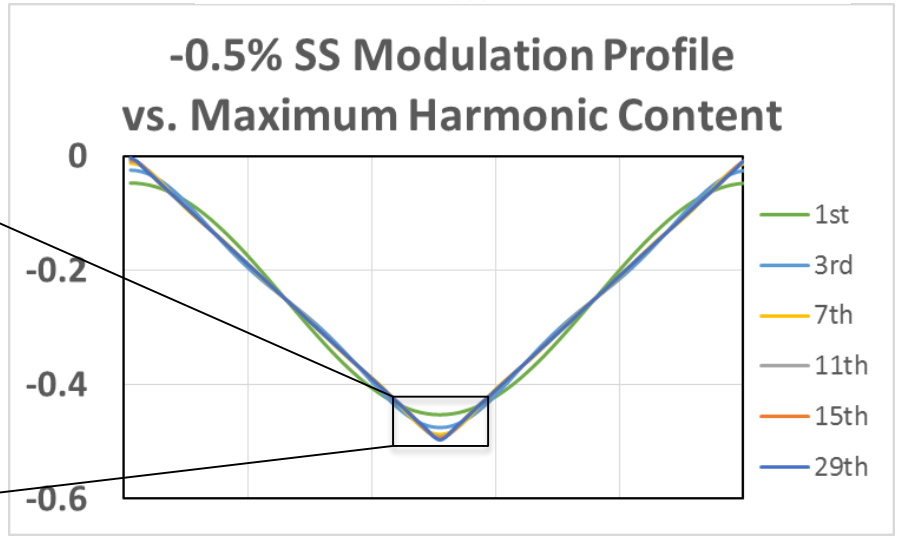


Jitter Attenuators

- **What if cascaded clock jitter exceeds spec?**
- **Can a jitter attenuator be used? "No"**
  - Bandwidth to pass spread passes jitter
  - Need the 29th harmonic (empirical), 928kHz = 32kHz x 29
  - Typical ZDB loop BW is 1-3MHz

$$f(x) = \left[\frac{4\,(0.5\%)}{\pi^2}\sum_{n=1,3,5,\ldots}^{\infty}\frac{(-1)^{(n-1)/2}}{n^2}\sin\left(\frac{n\pi x}{L}\right)\right] - \frac{0.5\%}{2}$$





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Accurate Jitter Measurements

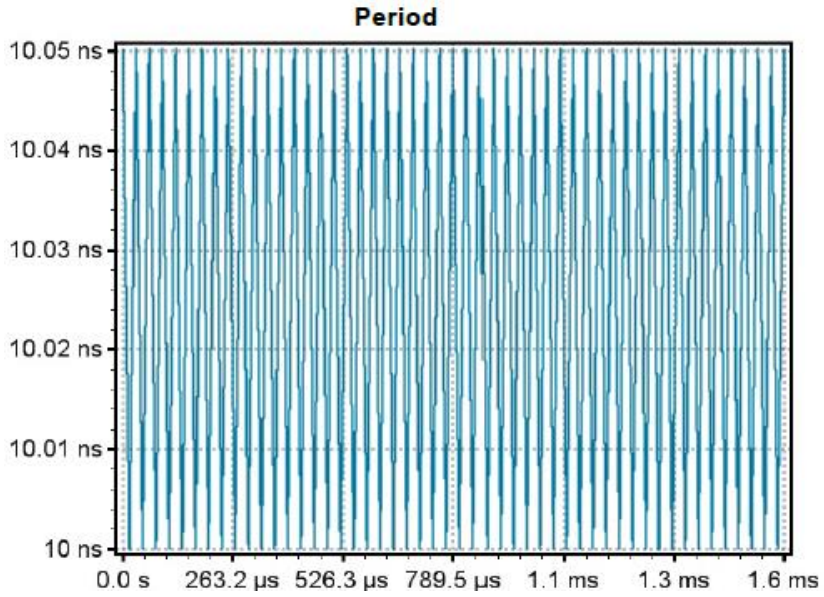
- **Use of sampling scope specified in standards**
  - Has higher noise than Phase Noise Analyzer (PNA)
  - But PNA does not lock to a spread signal
- **Typical sampling scope noise is -143dBc**
  - Results in ~250fs of jitter using Common Clock filter
  - Must be correlated out

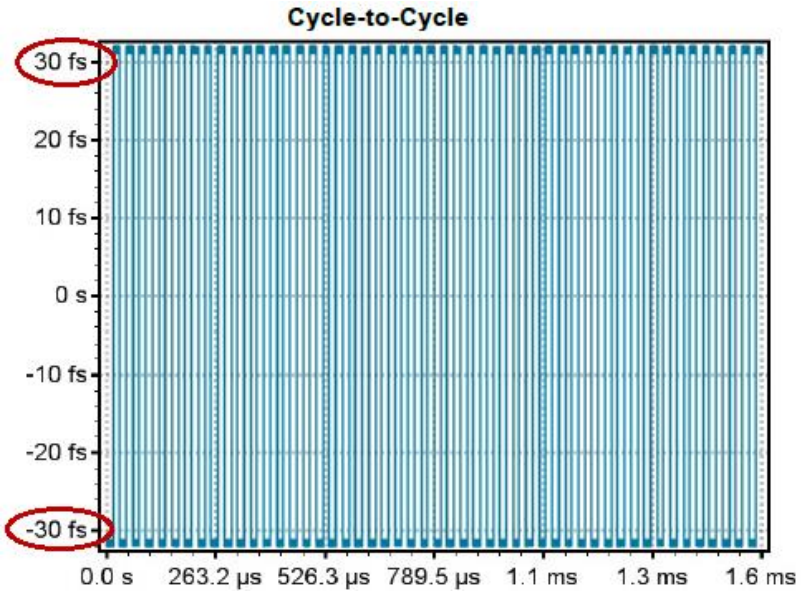
$$TIE = \sqrt{\left(\frac{Noise}{Slew\ Rate}\right)^2 + Intrinsic\ Jitter^2}\ [seconds\ peak]$$

NOTE: Effective scope jitter is a function of signal Tr/Tf

“Perfect SS Waveform”

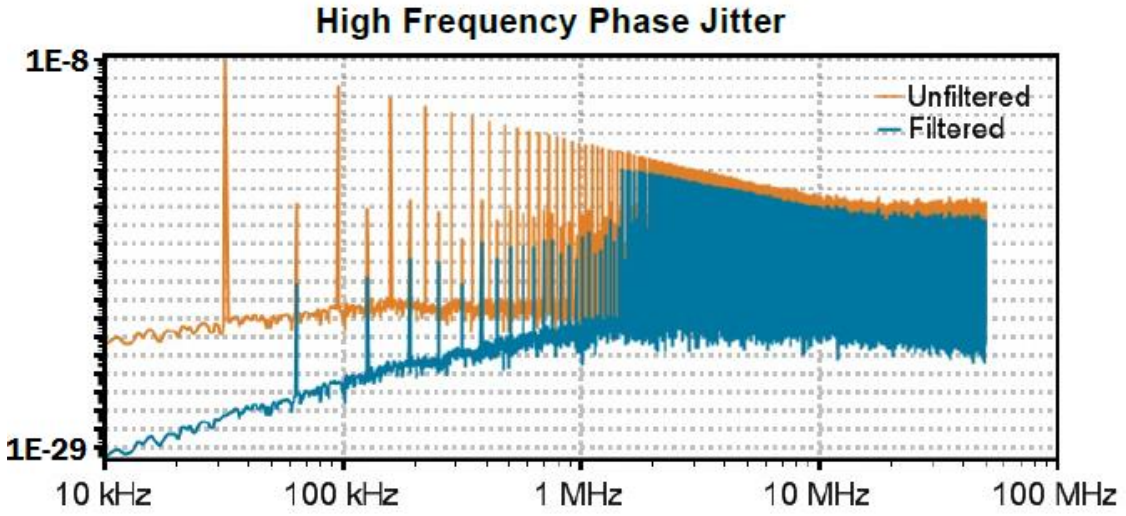
- **Mathematically generated**
- **Edge crossing rounded to 1fs**





“Perfect” SS Waveform Results

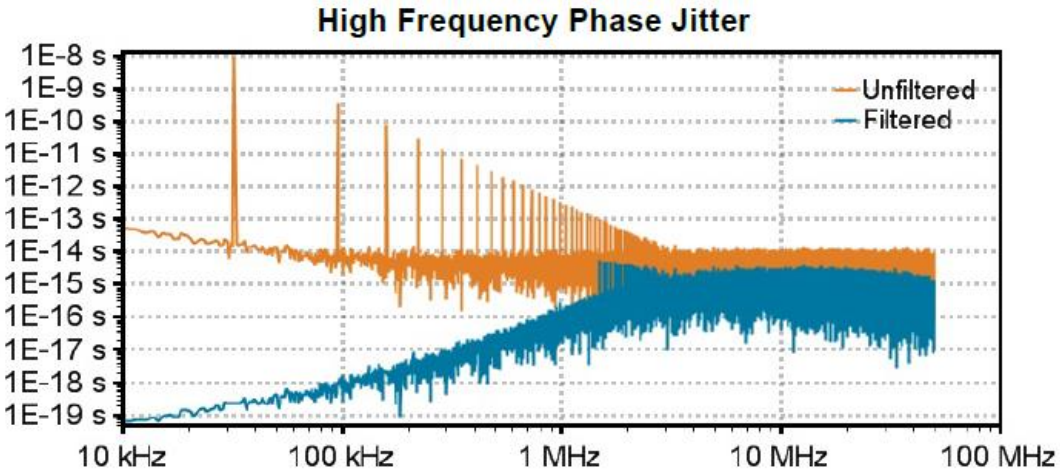
- **8&16GT/s CC**
  - 2M-2dB/5M-1dB
  - 23fs rms



Test	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	22.824 fs	PASS
Refclk LF RMS Jitter		8.102 fs	N/A
Pk-pk Phase Jitter		210.593 fs	N/A

Adding Typical Scope Noise

- **Added 1ps rms white noise**
  - Added to samples
  - Averaged during period interpolation
- **8&16GT/s CC**
  - 2M-2dB/5M-1dB
  - ~200fs rms
- **Must be rms subtracted from measurements**



Test	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	195.358 fs	PASS
Refclk LF RMS Jitter		5.382 fs	N/A
Pk-pk Phase Jitter		396.873 fs	N/A

Scope Noise Correction

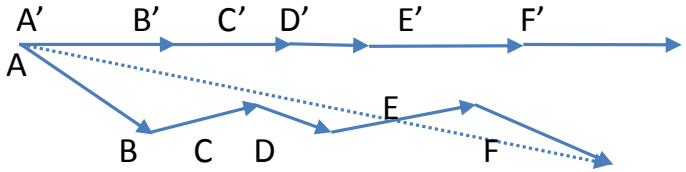
- **Compare to Phase Noise Analyzer (PNA)**
  - Measure non-spread with PNA
  - Measure non-spread with DSO
  - Calculate scope jitter = sqrt(J_{DSO}^2 – J_{PNA}^2)
  - Correlation factor required for each part type and setup
    - Scope jitter = $\sqrt{\left(\frac{Noise}{Slew\ rate}\right)^2 + Sample\ Clock\ Jitter^2}$
- **PNA does not include phase information for each frequency bin**
  - O.K. since integration will sum all phase worst case
    - See next slide

PNA PCIe Measurement

- **Filter PNA noise**
  - Multiply frequency bin magnitude by PCIe filter magnitude
  - Magnitude information preserved without phase
    - Complex numbers multiply magnitude and add phase angle
- **Integrate PNA noise**
  - Sum (magnitude) x (frequency bin BW)
  - Conservative measure of integrated noise
    - Complex integration sums real and imaginary parts

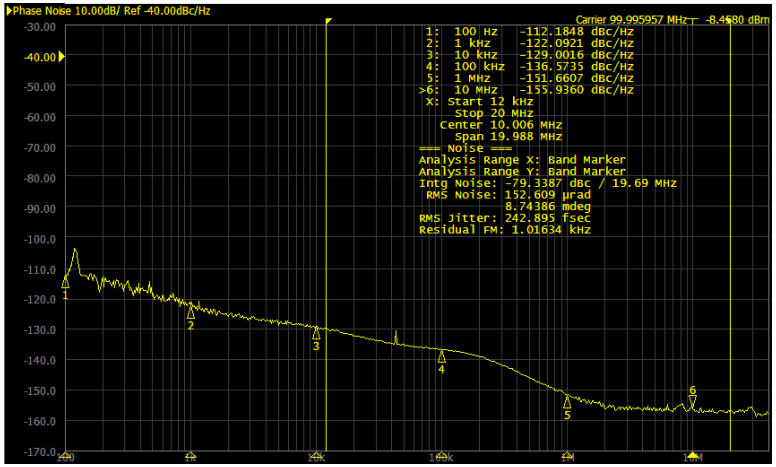
$$\int_a^b (u(t) + iv(t))\, dt = \int_a^b u(t)\, dt + i\int_a^b v(t)\, dt.$$

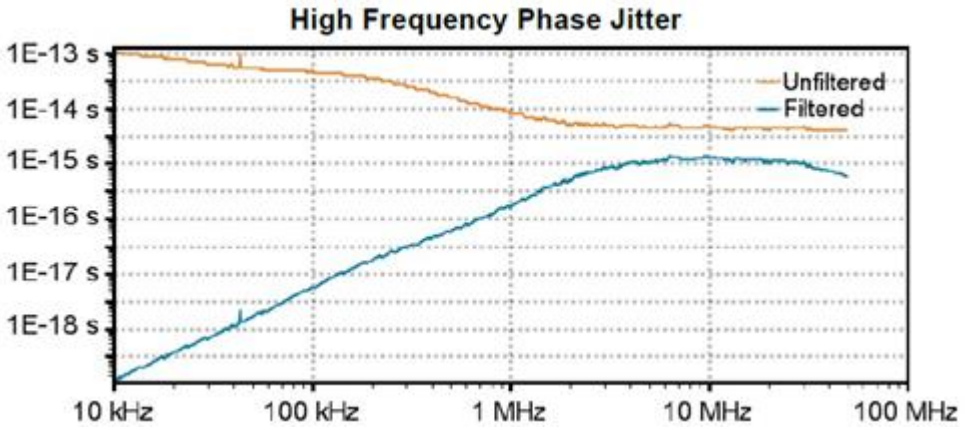
    - Summing magnitude only, A'-F'



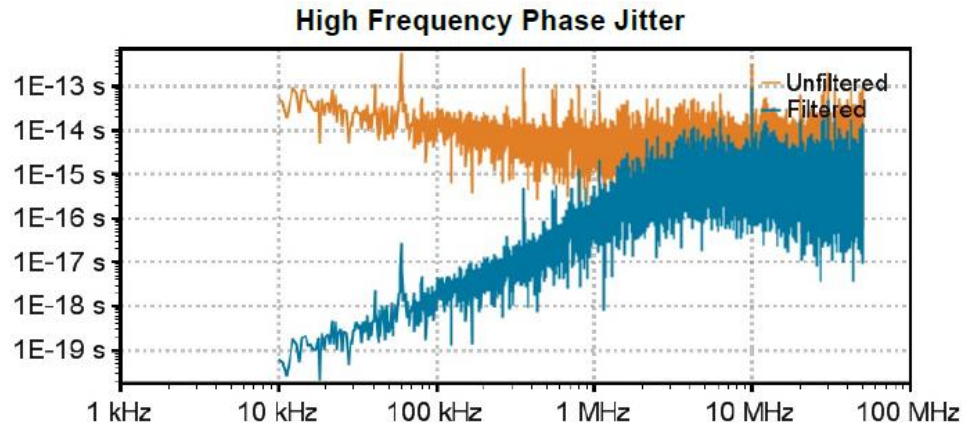
    - Summing magnitude and phase, A-F
    - Magnitude of A'-F' is always larger than A-F
      - |A'-F'| >,= |A-F|

Example Scope Noise Correction





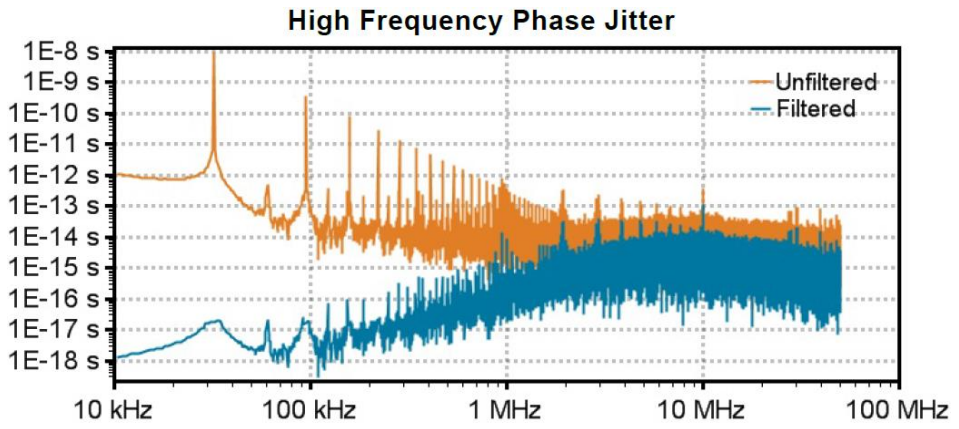
- **PNA results**
  - 0.05 ps rms
- **DSO results**
  - 4MHz/2dB,5MHz/0.01dB
  - 0.28 ps rms
  - 0.27 ps rms scope noise
    = sqrt (0.28^2 – 0.05^2)



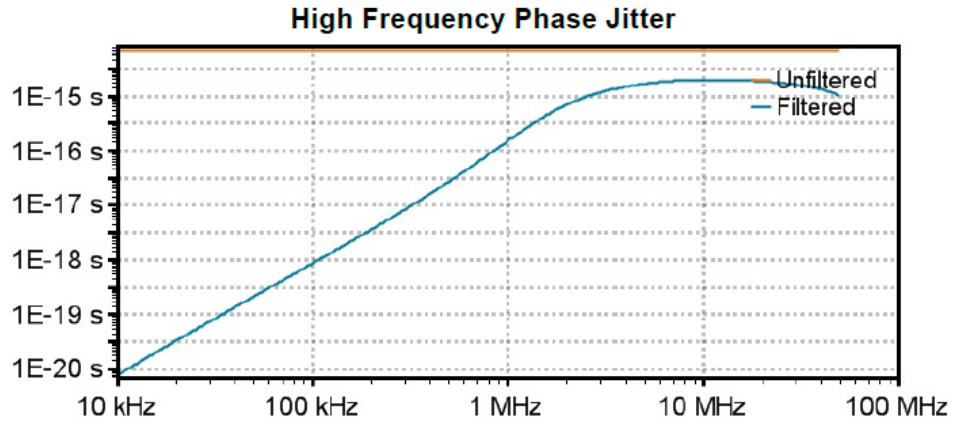
Apply to Spread Signal

- **DSO results**
  - 4MHz/2dB,5MHz/0.01dB
  - 0.39ps
  - 0.28ps Actual

    =sqrt(0.39^2 - 0.27^2)



- **DSO noise corresponds to**
  - -143dBc noise floor
  - 0.25ps integrated

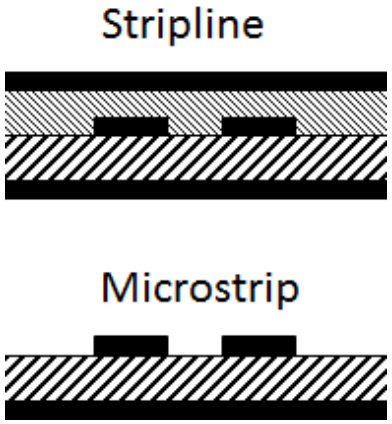


Agenda

- **Clock Architectures and Jitter Filters**
  - Common Clock (CC)
  - Separate Reference (SRIS/SRNS)
- **Clock Jitter Budgets**
  - 8GT/s
  - 16GT/s
- **Clock Fanout Architectures**
  - Single Plane or Connector
  - Cascaded Connector
- **Cascading Buffers**
  - Zero Delay Buffers
  - Fixed Delay Buffers
- **Accurate Jitter Measurements**
  - Sampling Scope Noise
  - Phase Noise Analyzer
- **Optimized Clock Routing**
  - Microstrip vs. Stripline
  - Long Trace Signal Integrity
  - Coupled Noise
- **Conclusion**

Clock Routing

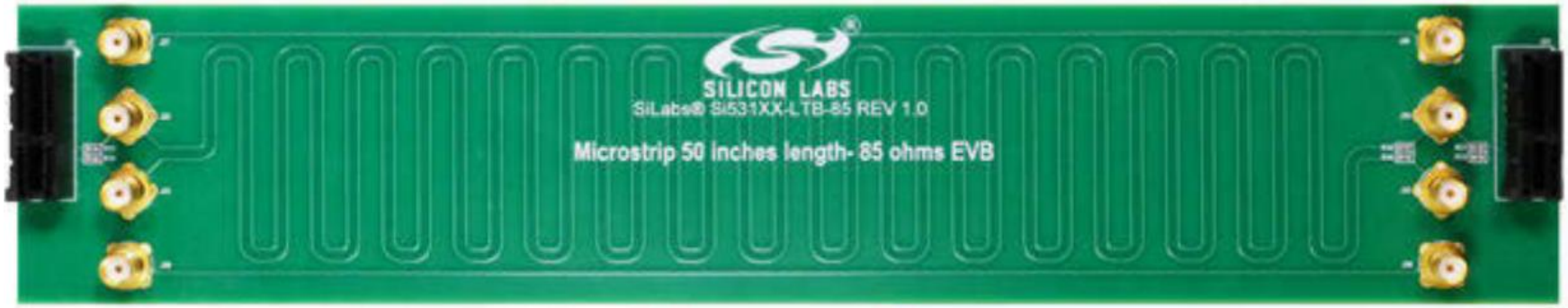
- **Microstrip vs. stripline**
  - Stripline provides better ambient shielding
  - Stripline requires vias (discontinuity)
- **12ns Tdelay is ~66in to 80in**
  - At 180ps/in stripline or 150ps/in microstrip
  - Channel length plus delta clock route
    - Trace plus buffer delay
- **Length reduces amplitude and slew**
  - Increases sensitivity to coupled noise
  - Increases buffer input additive rms jitter



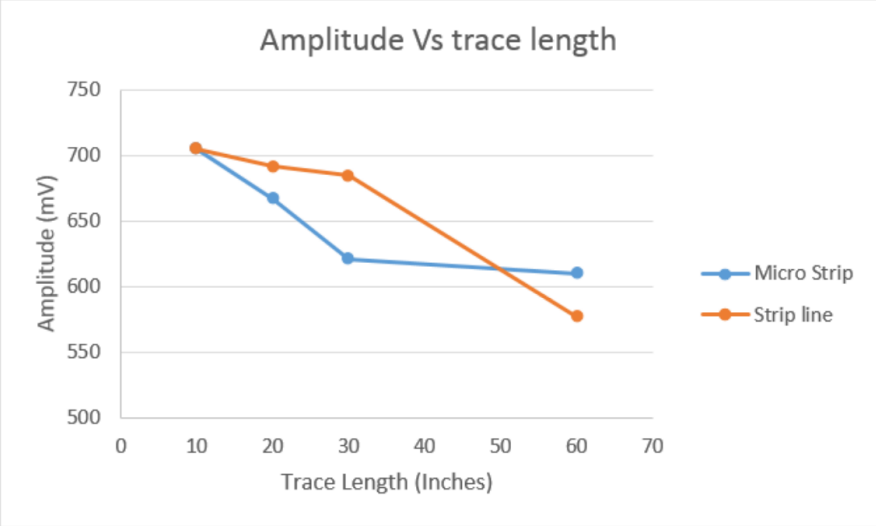
Impedance Discontinuities

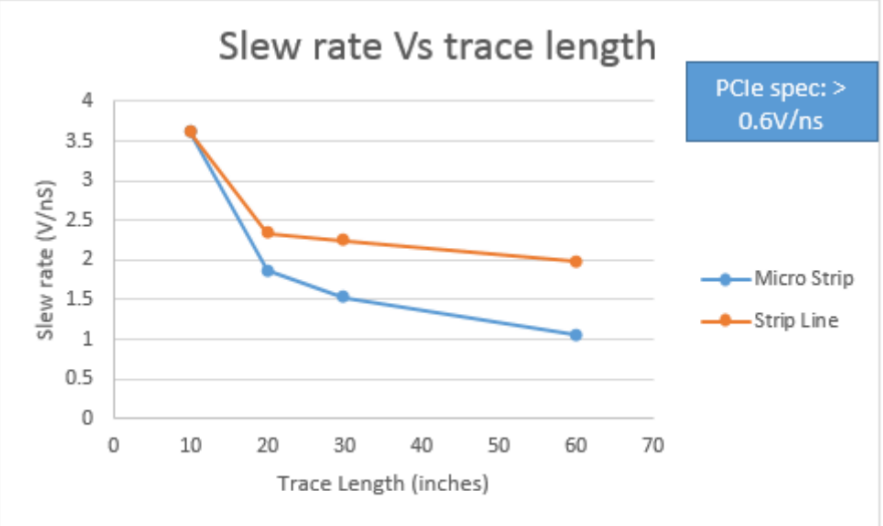
- **Trace vias and/or connectors**
  - Reflect energy that can distort (slow) edges
- **Avoid discontinuities located at**
  - Multiples of (half period) / (edge velocity) /2
- **Example via/connector ‘keep out’ region**
  - n x 14in ± 1.4 in (= 5ns/180ps/in /2 ± 10%)
  - Measured from launch point
  - +/-10% for modelling and manufacturing inaccuracy

Measured Clock SI

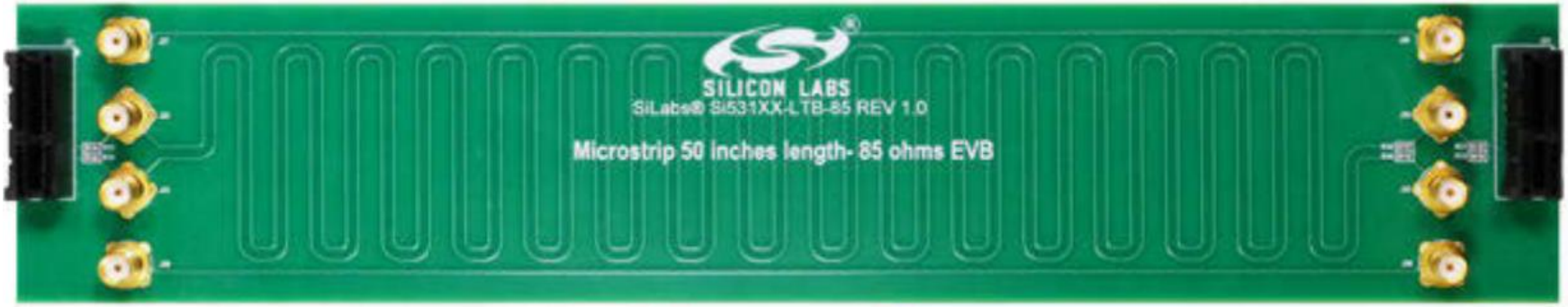


- 85 ohm trace segments with aggressors on exterior
- Connected to 10” trace eval boards through SMA/cable





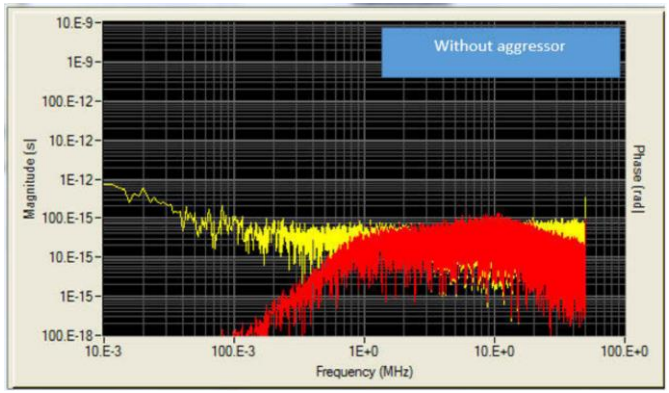
Example Aggressor

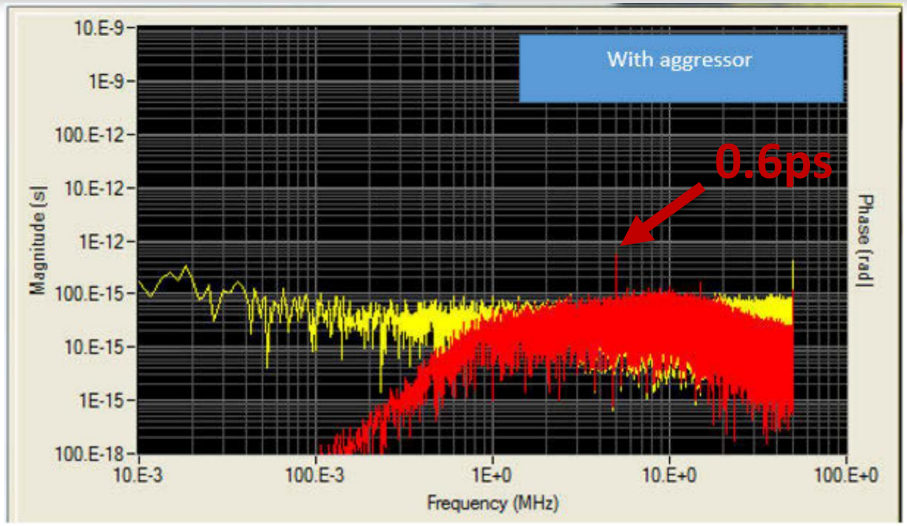


- **Two 105MHz, 3.3V single ended signals**
  - Walks phase in 20 cycles
- **Deterministic coupling**
  - Adds to ptp directly
  - Adds to rms scaled by $\frac{1}{sqrt(2)}$

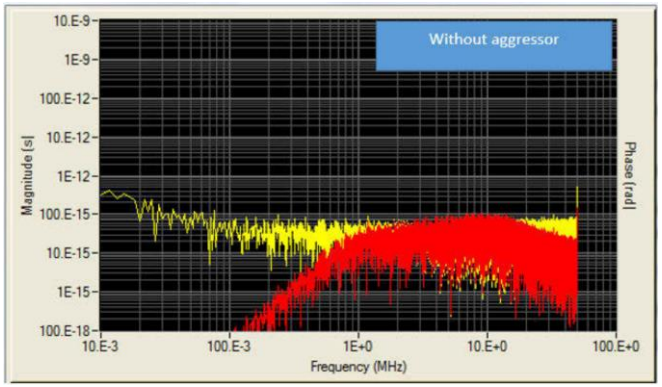
Resulting Crosstalk

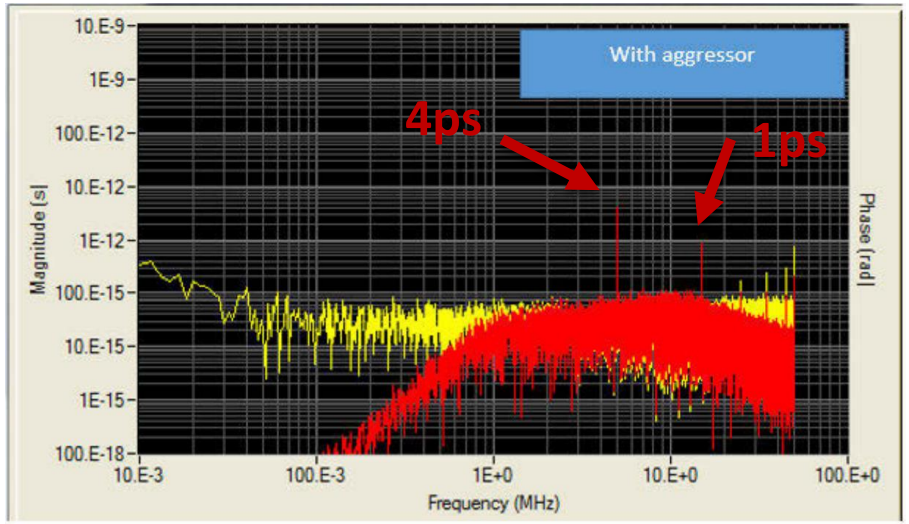
- **Stripline**





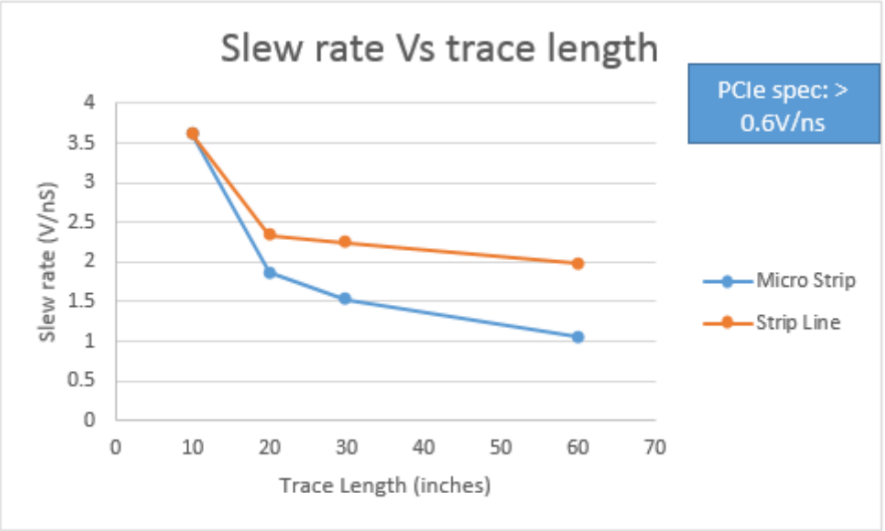
- **Microstrip**

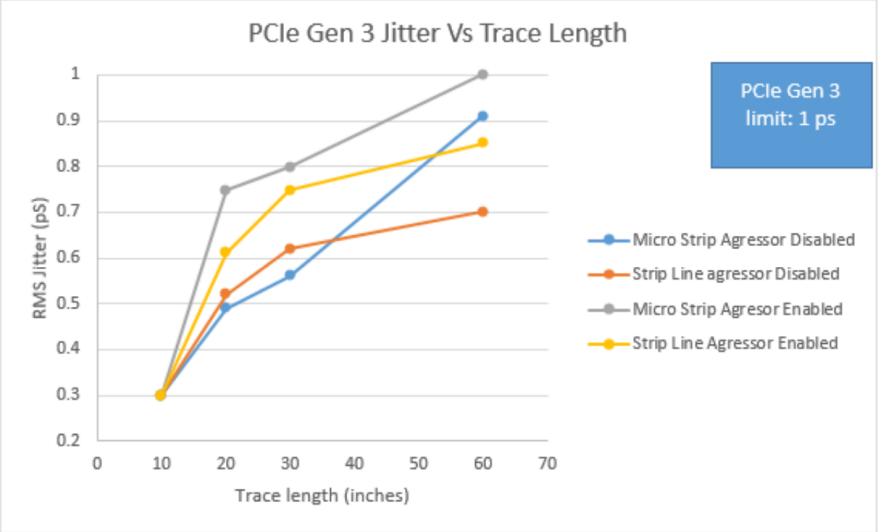




PCIe Jitter Results

- **Slower edge rates magnify scope and coupled noise jitter**
  - Coupled noise should be added to ptp but jitter tools add it rms
- **Microstrip more susceptible to RF ambients**





Conclusion

- **Cascading buffers for high clock fanout requires careful ptp jitter budgets**
  - rms and deterministic
  - ZDB filtering plus Tdelay may provide margin
- **Jitter attenuators are not an option**
  - Need to pass SS in common clock
- **Distribute buffers evenly when possible**
  - Restores slew and amplitude reducing noise sensitivity
- **Long traces require protection**
  - Adjacent ground shield or extra spacing
  - Stripline is better shielded from ambient (RF) noise
  - Avoid reflected energy coincident with edge launch

Acknowledgements

- **Harihara Subramanian – for experimental board design and extensive lab measurements**
  - SiLabs AN874: Cascading two Si53112 Buffers
  - SiLabs AN951: Driving Long Traces on PCIe Backplanes for Simple Evaluation

Thank you for attending the PCI-SIG Developers Conference 2017.

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